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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/602,111	06/23/2003	Hyang Ja Yang	SAM-0392	8471

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EXAMINER	
NGUYEN, DANG T	
ART UNIT	**PAPER NUMBER**
2824	

DATE MAILED: 08/10/2004

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/602,111	YANG ET AL.	
	Examiner	Art Unit	
	Dang T Nguyen	2824	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *23 June 2003*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-36* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1,2,8-23 and 32-36* is/are rejected.

7)☒ Claim(s) *3-7 and 24-31* is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *23 June 2003* is/are: a)☐ accepted or b)☒ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☒ All b)☐ Some * c)☐ None of:

1.☒ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date *6/23/03*.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☒ Other: *Search history*.

DETAILED ACTION

1. This action is responsive to the following communications: the Application and the Information Disclosure Statement filed on June 23, 2003.

2. Claims 1 – 36 are pending in this case. Claims 1 and 22 are independent claims.

Drawings

3. Figures 1 – 3 and 4A – 4C should be designated by a legend such as --Prior Art-- because only that which is old is illustrated. See MPEP § 608.02(g). Corrected drawing sheets are required in reply to the Office action to avoid abandonment of the application. The replacement sheet(s) should be labeled "Replacement Sheet" in the page header (as per 37 CFR 1.84(c)) so as not to obstruct any portion of the drawing figures. If the changes are not accepted by the examiner, the applicant will be notified and informed of any required corrective action in the next Office action. The objection to the drawings will not be held in abeyance.

Claim Rejections - 35 USC § 102

4. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (a) the invention was known or used by others in this country, or patented or described in a printed publication in this or a foreign country, before the invention thereof by the applicant for a patent.

Claims 1, 2, 16, 17, 20, 21, 22, 23, 32, 33 and 36 are rejected under 35 U.S.C. 102(a) as being anticipated by Applicant Admitted Prior Art (AAPA).

Regarding independent claim 1, Fig. 1 of AAPA discloses semiconductor memory device, comprising: a plurality of first memory arrays (MAT0, MAT2, MAT4, MAT6), a quantity of the first memory arrays being an even number arrays (MAT0, MAT2, MAT4, MAT6); a single second memory array (MAT1 or MAT3 or MAT5 or MAT7) comprising a plurality of memory blocks (Fig. 2 [Blk0 ... Blk7]); and a control circuit (MRD, Y-DEC& Y-GATE) associated with each of the first and second memory arrays, the control circuit generating control signals and providing the control signals to the first and second memory arrays such that data is input and output to and from the semiconductor memory device in multiples of nine bits (AAPA, Page 1 lines 18 – 24).

Regarding dependent claim 2, AAPA discloses wherein the control signals are sense amplifier control signals, the sense amplifier control signals selectively activating sense amplifiers in the memory arrays (page 1 line 25 – page 2 line 4).

Regarding dependent claim 16, AAPA discloses wherein each memory array comprises eight memory blocks and each memory block (Fig. 2 Blk0 – Blk7) comprises eight memory segments (Fig. 3 IO0 – IO7).

Regarding dependent claims 17, AAPA discloses wherein all of the plurality of memory arrays have the same input/output operational configuration (Fig. 2, AAPA page 1 lines 13-22).

Regarding dependent claim 20, AAPA discloses wherein the memory arrays comprise a plurality of first memory arrays, which are selectively activated during a read or write operation and a second memory array, which is activated by the control signals during every read or write operation (Fig. 4, AAPA page 2 lines 18 – 22).

Regarding dependent claim 21, AAPA discloses wherein the memory arrays all has the same memory density (Fig. 4A [X9]).

Regarding independent claim 22, Fig. 1 of AAPA discloses a method of processing data in a semiconductor memory device, comprising: providing a plurality of first memory arrays (MAT0, MAT2, MAT4, MAT6), a quantity of the first memory arrays being an even number (MAT0, MAT2, MAT4, MAT6); providing a single second memory array (MAT1 or MAT3 or MAT5 or MAT7) comprising a plurality of memory blocks (Fig. 2 [Blk0 ... Blk7]); and generating control signals (Fig. 2 [W/L, B/L]) and providing the control signals to the first and second memory arrays such that data is input and output to and from the semiconductor memory device in multiples of nine bits (AAPA, Page 1 lines 18 – 24).

Regarding dependent claim 23, AAPA discloses wherein the control signals are sense amplifier control signals, the sense amplifier control signals selectively activating sense amplifiers in the memory arrays (page 1 line 25 – page 2 line 4).

Regarding dependent claim 32, AAPA discloses wherein each memory array comprises eight memory blocks and each memory block (Fig. 2 Blk0 – Blk7) comprises eight memory segments (Fig. 3 IO0 – IO7).

Regarding dependent claim 33, AAPA dislcoses wherein all of the plurality of memory arrays has the same input/output operational configuration (Fig. 2, AAPA page 1 lines 13-22).

Regarding dependent claim 36, AAPA discloses wherein the memory arrays comprise a plurality of first memory arrays, which are selectively activated during a read

or write operation and a second memory array, which is activated by the control signals during every read or write operation (Fig. 4, AAPA page 2 lines 18 – 22).

Claim Rejections - 35 USC § 103

5. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

Claims 8 – 15, 18, 19, 34, and 35 are rejected under 35 U.S.C. 103(a) as being unpatentable over AAPA in view of Kobayashi et al. U.S. Patent No. 5,914,907 – filed Jul. 27, 1998.

Regarding dependent claims 8, 9, and 10, AAPA as applied above, disclosed every aspect of claim 1 invention, however AAPA fails to disclose wherein the memory arrays are arranged in three columns and three rows (claimed 8); a third memory array redundant to at least one of the first and second memory arrays (claimed 9); wherein the at least one of the first and second memory arrays is divided in half (claimed 10).

Fig. 1 of Kobayashi et al. disclose a memory arrays are arranged in three columns and three rows (Col. 5 lines 31 – 32); a third memory array redundant (62, 64) to at least one of the first and second memory arrays (2's, 6); wherein the at least one of the first and second memory arrays is divided in half (Fig. 1 discloses each memory 2 or 4 or 6 is divided in half by peripheral circuit 66, 68).

AAPA and Kobayashi et al. are common subject matter for memory arrays. Therefore it would have been obvious to one having ordinary skill in the art at the time the invention was made to incorporate the memory array arrangement taught by Kobayashi et al. to the memory arrays of AAPA for the purpose of providing a memory device capable of replacing with a redundant circuit while maintaining its rapid operation, restricting the increment in power consumption in the stand by operation, increases chip yield and also provides high reliability (Kobayashi et al., Col. 2 lines 55 – 65).

Regarding to claims 11, 12, and 13, AAPA modified by Kobayashi et al. as applied to claim 8 above, disclosed every aspect of claimed invention, however AAPA fails to disclose a peripheral circuit is formed on the semiconductor memory device (claimed 11); wherein the peripheral circuit is formed dividing at least one of the first and second memory arrays (claimed 12); and wherein the at least one of the first and second memory arrays is divided in half (claimed 13).

Fig. 1 of Kobayashi et al. further discloses a peripheral circuit (66,68 row decoder) is formed on the semiconductor memory device; wherein the peripheral circuit ([66,68] row decoder) is formed dividing at least one of the first and second memory arrays (2, 4 or 6); and wherein the at least one of the first and second memory arrays is divided in half ([66,68] row decoder divided each of memory arrays 2, 4, 6 into half and forming two main memory cells for each memory array. See Fig. 1 of Kobayashi et al.).

AAPA and Kobayashi et al. are common subject matter for memory arrays. Therefore it would have been obvious to one having ordinary skill in the art at the time

the invention was made to incorporate the memory array arrangement taught by Kobayashi et al. to the memory arrays of AAPA for the purpose of providing subblock-by-subblock replacement of regular memory cell arrays with a redundant memory cell array to optimizing chip area, and memory cell arrays can be use as equivalent memory cell arrays to achieve x 9 configuration, and provide an efficient error detection and hence a highly reliable memory (Kobayashi et al., Col. 4 lines 11 - 37).

Regarding dependent claims 14 and 15, AAPA modified by Kobayashi et al. as applied to claimed 8 above, however AAPA fails to disclose a third memory array redundant to at least one of the first and second memory arrays (claimed 14); and a peripheral circuit formed on the semiconductor memory device (claimed 15).

Fig. 1 of Kobayashi et al. discloses a third memory array redundant (62, 64) to at least one of the first and second memory arrays (2's, 6); and a peripheral circuit (66,68 row decoder) formed on the semiconductor memory device; wherein the third memory array (62, 66) and the peripheral circuit (66, 68) are formed dividing at least one of the first and second memory arrays (Kobayashi, Fig. 1).

AAPA and Kobayashi et al. are common subject matter for memory arrays. Therefore it would have been obvious to one having ordinary skill in the art at the time the invention was made to incorporate the memory array arrangement taught by Kobayashi et al. to the memory arrays of AAPA for the purpose of providing subblock-by-subblock replacement of regular memory cell arrays with a redundant memory cell array to optimizing chip area, and memory cell arrays can be use as equivalent memory

cell arrays to achieve x 9 configuration, and provide an efficient error detection and hence a highly reliable memory (Kobayashi et al., Col. 4 lines 11 - 37).

Regarding dependent claims 18 and 34, AAPA as applied above, disclosed every aspect of claims 1 and 22 invention, however AAPA fails to disclose wherein the quantity of memory arrays is nine.

Fig. 1 of Kobayashi et al. discloses wherein the quantity of nine memory arrays.

AAPA and Kobayashi et al. are common subject matter for memory arrays. Therefore it would have been obvious to one having ordinary skill in the art at the time the invention was made to incorporate the memory array arrangement taught by Kobayashi et al. to the memory arrays of AAPA for the purpose of providing subblock-by-subblock replacement of regular memory cell arrays with a redundant memory cell array to optimizing chip area, and memory cell arrays can be use as equivalent memory cell arrays to achieve x 9 configuration, and provide an efficient error detection and hence a highly reliable memory (Kobayashi et al., Col. 4 lines 11 - 37).

Regarding dependent claims 19 and 35, AAPA as applied above, disclosed every aspect of claims 1 and 22 invention, however AAPA fails to disclose wherein the quantity of memory arrays is an integer multiple of nine.

Fig. 1 of Kobayashi et al. discloses the memory device having quantity of memory arrays is an integer multiple of nine (which can be 9 memory arrays or 18 of main memory cell block; therefore fig. 1 having integer (1or 2) multiple of nine quantity of memory.

AAPA and Kobayashi et al. are common subject matter for memory arrays. Therefore it would have been obvious to one having ordinary skill in the art at the time the invention was made to incorporate the memory array arrangement taught by Kobayashi et al. to the memory arrays of AAPA for the purpose of providing subblock-by-subblock replacement of regular memory cell arrays with a redundant memory cell array to optimizing chip area, and memory cell arrays can be use as equivalent memory cell arrays to achieve x 9 configuration, and provide an efficient error detection and hence a highly reliable memory (Kobayashi et al., Col. 4 lines 11 - 37).

Allowable Subject Matter

6. Claims 3 – 7 and 24 - 31 objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims.

7. The following is a statement of reasons for the indication of allowable subject matter:

With respect to claims 3 and 24, the prior art AAPA and '907' do not teach a semiconductor memory array device having one of the memory arrays is associated with a quantity of bits of one of one, two, four and eight bits, depending on a data input/output operational configuration of the memory device.

With respect to claims 4 and 25, the prior art AAPA and '907' do not teach a semiconductor memory array device having: in a by-nine operational configuration,

each of two of the first memory arrays is associated with four bits, and the second memory array is associated with a single bit.

With respect to claims 5 and 26, the prior art AAPA and '907' do not teach a semiconductor memory array device having: in a by-eighteen operational configuration, each of four of the first memory arrays is associated with four bits, and the second memory array is associated with two bits.

With respect to claims 6 and 27, the prior art AAPA and '907' do not teach a semiconductor memory array device having: in a by-thirty-six operational configuration, each of four of the first memory arrays is associated with eight bits, and the second memory array is associated with four bits.

With respect to claims 7 and 28, the prior art AAPA and '907' do not teach a semiconductor memory array device having: in a by-seventy-two operational configuration, each of eight of the first memory arrays is associated with eight bits, and the second memory array is associated with eight bits.

With respect to claim 29, the prior art AAPA and '907' do not teach a semiconductor memory array device having: in a by-nine operational configuration, each of the first memory arrays and the second memory array is associated with one bit of data.

With respect to claim 30, the prior art AAPA and '907' do not teach a semiconductor memory array device having: in a by-eighteen operational configuration, each of the first memory arrays and the second memory array is associated with two bits of data.

With respect to claim 31, the prior art AAPA and '907' do not teach a semiconductor memory array device having: in a by-thirty-six operational configuration, each of the first memory arrays and the second memory array is associated with four bits of data.

Prior art

8. The prior art made of record and not relied upon is considered pertinent to applicant's disclosure.

Amano et al.	Patent No. US 6,072,743	Date of Patent: Jun. 6, 2000
Kokubo	Patent No. US 5,706,231	Date of Patent: Jan. 6, 1998
Kim	Patent No. US 6,694,422 B1	Date of Patent: Feb. 17, 2004

Contact Information

9. Any inquiry concerning this communication from the examiner should be directed to Dang Nguyen, who can be reached by telephone at ~~(703) 305-1673~~ 571-272-1955. Normal contact times are M-F, 8:00 AM - 4:30 PM.

Upon an unsuccessful attempt to contact the examiner, the examiner's supervisor, Richard Elms, may be reached at (571) 272-1869.

Any inquiry of a general nature or relating to the status of this application or proceeding should be directed to the receptionist, whose telephone number is (703)

305-3900. The faxed phone number for organization where this application or proceeding is assigned is (703) 872-9306.

Information regarding the Status of an application may be obtained from the patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free) or EBC@uspto.gov.

Dang Nguyen 8/4/2004

8/9/04

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